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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,657	CHOU, MIN-CHUNG	
	Examiner	Art Unit	
	Pho M. Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed on 10/13/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-13 and 17-24* is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Reply to Election/Restrictions

1. Applicant's election without traverse of Group I, Claims 1-13 and 17-24 filed 13 October 2005 is acknowledged. The changes and remarks disclosed therein were considered.

2. Claims 14-16 have been canceled.

3. Claims 1-13 and 17-24 are pending in the application.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it uses the phrase **"described"** in line 2, which is implied. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 and 3-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakano. (US. 6,005,815).

Regarding claim 1, Nakano in Figure 1 and Figure 5 discloses a memory device for burn in test, the memory device comprising:

an array of memory cells ($MC30_{1,n}$ $MC30_{2,n}$ $MC30_{m,n}$ Figure 1), a plurality of word lines (WL1, WL2, WL_m, Figure 1), each word line connected to a column of the array of memory cells (gate of each memory cells $MC30_{1,n}$ $MC30_{2,n}$ $MC30_{m,n}$ connected WL1, WL2 and WL_m); and

a leak current limited unit (transistors 28 and 29 in Figure 5) connected to the array of memory cells ($MC30_{1,n}$ $MC30_{2,n}$ $MC30_{m,n}$ Figure 1) via the plurality of word lines (WL1, WL2, WL_m, Figure 1);

wherein during the burn in test (low TEST signal 21, Figure 5), the leak current limited unit limits the current (transistors 28 and 29 in Figure 5) in each word line (WL1, WL2, WL_m, Figure 1) to a predetermined word line current value (current corresponding

to 7volts and 0 volts, see column 5, lines 50-55) and a word line stress voltage (VT1, VT2, Figure 5) is provided via the leak current limited unit to stress each of column of memory cells connected to one word line (see column 5, lines 40-55).

With respected to claim 3, Nakano in Figure 1 and Figure 5 discloses the memory device wherein the leak current limited unit (transistors 28 and 29 in Figure 5) including a plurality of single word line leak current limited unit (transistor 28 in Figure 5 is a single current limited unit) wherein each single word line leak current limited unit is connected to one word line (transistor 28 coupled to $MC30_{1,n}$ through WL1 in Figure 1) and limits the current in the word line to the predetermined word line current value (current corresponding to 7volts and 0volts, see column 5, lines 50-55).

With respected to claim 4, Nakano in Figure 5 discloses the memory device wherein the single word line leak current limited unit is a MOS transistor (transistor 28 is PMOS, see column 6, line 12).

With respected to claim 5, Nakano in Figure 1 and Figure 5 discloses the memory device wherein the leak current limited (transistors 28 and 29 in Figure 5) including a plurality of sub-array word line leak current limited units (transistors 28 and 29), wherein each sub-array word line leak current limited unit is connected to a number of word line (transistor 28 coupled to $MC30_{1,n}$ through WL1 in Figure 1) and limits the total current flowing through the number of word lines to a predetermined sub-array current value (current corresponding to 7V and 0V, see column 5, line 50-55).

With respected to claim 6, Nakano in Figure 5 discloses the memory device wherein the sub-array word line leak current limited unit comprises at least one level shifter (28, 29, Figure 5) and each level shifter is used to limit current.

With respected to claim 7, Nakano in Figure 5 discloses the memory device wherein the leak current limited unit (transistors 28 and 29 in Figure 5) including a plurality of single word line leak current limited units (28, 29, Figure 5), the sub-array word line leak current limited units are connected to the word lines (transistor 28 coupled to $MC30_{1,n}$ through WL1 in Figure 1) via the single word line leak current limited units and each single word line leak current limited unit is connected to one word line and limits the current in the word line to the predetermined word line current value (current corresponding to 7V and 0V, see column 5, line 50-55).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano. (US. 6,005,815) as applied to claim 1 above, and further in view of Fujita. (US. 5,293,340).

Regarding to claim 2. Nakano teaches a memory device having all the basic limitations of the claimed invention, and further including memory cells for access

transistor. However, Nakano fails to explicitly mention the memory cell comprises an access transistor and a storage capacitor. Regardless, it is well known in the art that a volatile semiconductor memory device comprises an access transistor and a storage capacitor.

Fujita teaches a DRAM memory device (1, Figure 1, column 2, lines 21-26). Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the memory device of Nakano with the aforementioned teaching of Fujita. since it is known in the art that the DRAM semiconductor memory device would include memory cell as an access transistor and storage capacitor.

Allowable Subject Matter

9. Claims 8-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 8, the prior art of record do not disclose or suggest the current value sum is a sum of the first current value and a second current values and the second current value is the current value an additional spare word line is capable of supporting.

Regarding claim 9, the prior art of record do not disclose or suggest the total current flowing into the memory device is limited to a predetermined total current is less

than the maximum current value a voltage source is capable of providing and the voltage source provides the word line stress voltage to the memory device.

10. Claims 10-13 and 17-24 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to provide:

"applying a predetermined high voltage to the source of the first PMOS transistor so that both of the source of the first PMOS transistor and the second PMOS transistor are kept at the predetermined high voltage and providing a predetermined low voltage to the output of the word line driver via a word line" in a method for keeping the output of a word line driver in high impedance state during a burn in test on a memory cell as claimed in the independent claim 10. Claim 11 is also allowed because of their dependency on claim 10; or

"in the normal mode, a read write operation of the row of memory cells connected to the bit line is performed via the normal data in path and in the burn in test mode, a bit line stress voltage serves as the input data and is applied to the row of memory cells via the burn in test path to perform the burn in test" in a switch circuit as claimed in the independent claim 12. Claim 13 is also allowed because of their dependency claim 12; or

"a plurality of switch circuits wherein each switch circuit is connected to one bit line and each switch circuit switches between a normal data in path and a burn in test path in the burn in test on a row of memory cells" in a memory device

for a burn in test as claimed in the independent claim 17. Claims 18-24 are also allowed because of their dependency claim 17.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Nguyen

PML
17 February 2006